ZMCIS372xC General Dual-Channel Digital Isolators

1 Key Features

- **Data rate: DC to 40Mbps**
- **Robust isolation barrier**
    - High lifetime: >40 years
    - Up to 5kV$_{RMS}$ isolation rating (wide-body packages)
    - ±150kV/µs typical CMTI
- **Wide supply range: 3.0V to 5.5V**
- **Wide operating temperature range: –40°C to 125°C**
- **No start-up initialization required**
- **Default output *High* (ZMCIS372xCH) and *Low* (ZMCIS372xCL) Options**
- **High electromagnetic immunity**
- **Low power consumption**
    - 2.6mA per channel at 1Mbps with V_{DDX} = 5.0V
    - 5.2mA per channel at 40Mbps with V_{DDX} = 5.0V
- **Best in class propagation delay and skew**
    - 22ns typical propagation delay
    - 3ns propagation delay skew (chip -to-chip)
    - 1ns pulse width distortion
    - 20ns minimum pulse width
- **Schmitt trigger inputs**
- **Package options**
    - Narrow-body SOIC8 (S) package
    - Wide-body SOIC8-WB (G) package
    - Wide-body SOIC16-WB (W) package
- **Safety regulatory approvals**
    - VDE 0884-17:2021-10 isolation certification
    - UL according to UL 1577
    - GB 4943.1-2022 certification

2 Applications

- Industrial Automation
- Motor Control
- Medical Systems
- Isolated Power Supplies
- Solar Inverters
- Isolated ADC, DAC

3 Description

The ZMCIS372xC devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS digital I/O. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier, and each channel input integrates Schmitt trigger to provide excellent noise immunity.

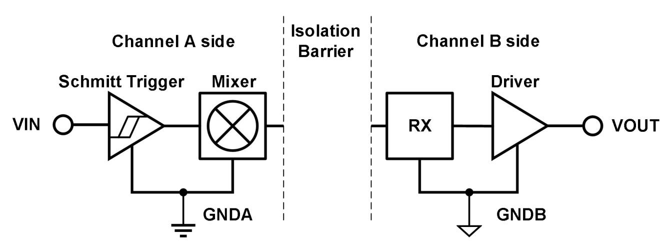
The ZMCIS3720C features two channels transferring digital signals in one direction for applications such as isolated digital I/O. The ZMCIS3721C/ZMCIS3722C devices have 2 channels with 1 channel in each direction, making them ideal for isolating the TX and RX lines of a transceiver, such as RS-485, CAN etc. communication. When the input is either not powered or open-circuit, the default output is low for devices with suffix L and high for devices with suffix H.

The ZMCIS372xC devices are specified over the –40°C to +125°C operating temperature range and are available in 8-pin narrow-body SOIC package (3.75kV$_{RMS}$, basic isolation), 8-pin or 16-pin wide-body SOIC package (5kV$_{RMS}$, reinforced isolation).

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ZMCIS3720C ZMCIS3721C ZMCIS3722C	SOIC8 (S)	4.90mm × 3.90mm
	SOIC8-WB (G)	5.80mm × 7.50mm
	SOIC16-WB (W)	10.30mm × 7.50mm

Simplified Channel Structure



GNDA and GNDB are the isolated grounds for A side and B side respectively.

4 Ordering Guide

Table 4- 1 Ordering Guide for Valid Ordering Part Number

Part Number	Number of Inputs A Side	Number of Inputs B Side	Default Output	Isolation Rating (kV_{RMS})	Package
ZMCIS3720CLS	2	0	Low	3.75	SOIC8 (S)
ZMCIS3720CLG	2	0	Low	5.0	SOIC8-WB (G)
ZMCIS3720CLW	2	0	Low	5.0	SOIC16-WB (W)
ZMCIS3720CHS	2	0	High	3.75	SOIC8 (S)
ZMCIS3720CHG	2	0	High	5.0	SOIC8-WB (G)
ZMCIS3720CHW	2	0	High	5.0	SOIC16-WB (W)
ZMCIS3721CLS	1	1	Low	3.75	SOIC8 (S)
ZMCIS3721CLG	1	1	Low	5.0	SOIC8-WB (G)
ZMCIS3721CLW	1	1	Low	5.0	SOIC16-WB (W)
ZMCIS3721CHS	1	1	High	3.75	SOIC8 (S)
ZMCIS3721CHG	1	1	High	5.0	SOIC8-WB (G)
ZMCIS3721CHW	1	1	High	5.0	SOIC16-WB (W)
ZMCIS3722CLS	1	1	Low	3.75	SOIC8 (S)
ZMCIS3722CLG	1	1	Low	5.0	SOIC8-WB (G)
ZMCIS3722CLW	1	1	Low	5.0	SOIC16-WB (W)
ZMCIS3722CHS	1	1	High	3.75	SOIC8 (S)
ZMCIS3722CHG	1	1	High	5.0	SOIC8-WB (G)
ZMCIS3722CHW	1	1	High	5.0	SOIC16-WB (W)

Table of Contents

5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2024.08.09	NA

6 Pin Descriptions and Functions

6.1 8-Pin SOIC Package

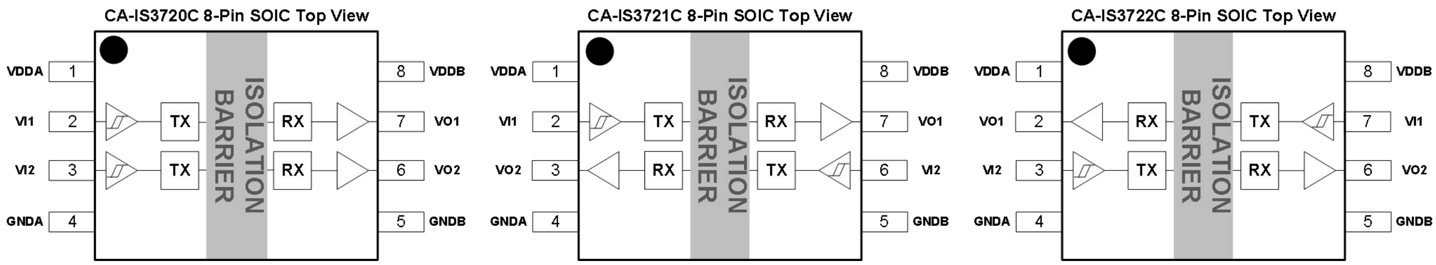


Figure 6- 1 ZMCIS372xC 8-Pin Narrow-body and Wide-body SOIC Packages (Top View)

Table 6- 1 Pin Description and Functions

SOIC8 PIN NUMBER			NAME	TYPE	DESCRIPTION
ZMCIS3720C	ZMCIS3721C	ZMCIS3722C			
1	1	1	VDDA	Supply	Power supply for side A.
2	2	7	VI1	Digital I/O	Digital input 1 on side A/B, corresponds to logic output 1 on side B/A.
3	6	3	VI2	Digital I/O	Digital input 2 on side A/B, corresponds to logic output 2 on side B/A.
4	4	4	GNDA	Ground	Ground reference for side A.
5	5	5	GNDB	Ground	Ground reference for side B.
7	7	2	VO1	Digital I/O	Digital output 1 on side B/A, VO1 is the logic output for the VI1 input on side A/B.
6	3	6	VO2	Digital I/O	Digital output 2 on side B/A, VO2 is the logic output for the VI2 input on side A/B.
8	8	8	VDDB	Supply	Power supply for Side B.

6.2 16-Pin SOIC Package

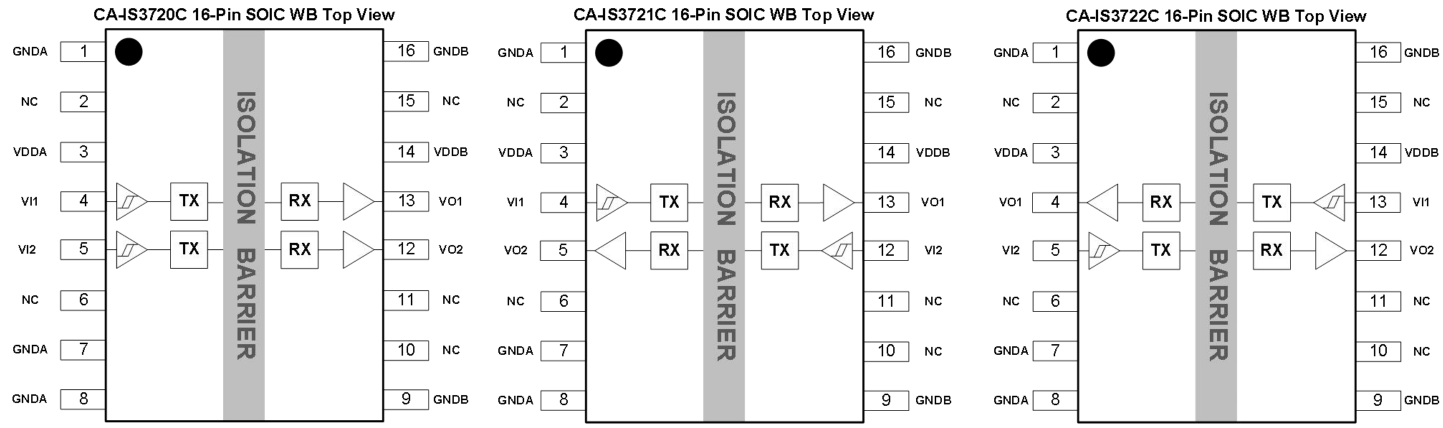


Figure 6- 2 ZMCIS372xC 16-Pin Wide-body SOIC Package (Top View)

Table 6- 2 Pin Description and Functions

SOIC-16 PIN NUMBER			NAME	TYPE	DESCRIPTION
ZMCIS3720C	ZMCIS3721C	ZMCIS3722C			
1, 7, 8	1, 7, 8	1, 7, 8	GNDA	Ground	Ground reference for side A.
2, 6	2, 6	2, 6	NC	No Connect	Not internally connected. They can be left floating, tied to VDDA or tied to GNDA.
3	3	3	VDDA	Supply	Power supply for side A.
4	4	13	VI1	Digital I/O	Digital input 1 on side A/B, corresponds to logic output 1 on side B/A.
5	12	5	VI2	Digital I/O	Digital input 2 on side A/B, corresponds to logic output 2 on side B/A.
10, 11, 15	10, 11, 15	10, 11, 15	NC	No Connect	Not internally connected. They can be left floating, tied to VDDB or tied to GNDB.
9, 16	9, 16	9, 16	GNDB	Ground	Ground reference for side B.
13	13	4	VO1	Digital I/O	Digital output 1 on side B/A, VO1 is the logic output for the VI1 input on side A/B.
12	5	12	VO2	Digital I/O	Digital output 2 on side B/A, VO2 is the logic output for the VI2 input on side A/B.
14	14	14	VDDB	Supply	Power supply for side B.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage[2]	–0.5	7.0	V
V_{IN}	Voltage at VIx	–0.5	V_{DDI} + 0.5[3]	V
I_O	Output current	–20	20	mA
T_J	Junction Temperature	–40	150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:
1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the local ground (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 7V.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pins at same side	±8	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±2	

7.3 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{DDA}, V_{DDB}	Supply voltage		3.0	3.3 or 5.0	5.5	V
$V_{DD\ (UVLO+)}$	V_{DDX} undervoltage-lockout threshold @ rising edge		2.55	2.7	2.85	V
$V_{DD\ (UVLO-)}$	V_{DDX} undervoltage-lockout threshold @ falling edge		2.35	2.5	2.65	V
$V_{HYS\ (UVLO)}$	V_{DDX} undervoltage-lockout threshold hysteresis		150	200	270	mV
I_{OH}	High-level output current	V_{DDO}[1] = 5V	-4			mA
		V_{DDO}[1] = 3.3V	-2			
I_{OL}	Low-level output current	V_{DDO}[1] = 5V			4	mA
		V_{DDO}[1] = 3.3V			2	
V_{IH}	High-level input voltage		0.7 × V_{DDI}[2]		V_{DDI}[2]	V
V_{IL}	Low-level input voltage		0		0.3 × V_{DDI}[2]	V
DR	Data rate		0		40	Mbps
T_A	Ambient temperature		-40	27	125	°C
T_J	Junction temperature		-40		150	°C

NOTE:
1. V_{DDO} = output-side supply V_{DD}.
2. V_{DDI} = input-side supply V_{DD}.

7.4 Thermal Information

THERMAL METRIC		PACKAGE			UNIT
		SOIC8 (S)	SOIC8-WB (G)	SOIC16-WB (W)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.0	92.3	83.4	°C/W

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ZMCIS3720C						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5V, C_L = 15pF, T_J = 150°C, Input a 20-MHz 50% duty cycle square wave			60	mW
P_{DA}	Maximum Power Dissipation on Side A				20	mW
P_{DB}	Maximum Power Dissipation on Side B				40	mW
ZMCIS3721C						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5V, C_L = 15pF, T_J = 150°C, Input a 20-MHz 50% duty cycle square wave			60	mW
P_{DA}	Maximum Power Dissipation on Side A				30	mW
P_{DB}	Maximum Power Dissipation on Side B				30	mW
ZMCIS3722C						
P_D	Maximum Power Dissipation	V_{DDA} = V_{DDB} = 5.5V, C_L = 15pF, T_J = 150°C, Input a 20-MHz 50% duty cycle square wave			60	mW
P_{DA}	Maximum Power Dissipation on Side A				30	mW
P_{DB}	Maximum Power Dissipation on Side B				30	mW

7.6 Insulation Specifications

PARAMETR		TEST CONDITIONS	VALUE		UNIT
			S	G/W	
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	4	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	4	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	28	28	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	> 600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ $300V_{RMS}$	I-III	I-IV	
		Rated mains voltage ≤ $600V_{RMS}$	NA	I-IV	
		Rated mains voltage ≤ $1000V_{RMS}$	NA	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	566	1414	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) Test	400	1000	V_{RMS}
		DC voltage	566	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1s (100% production)	5300	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	1.2/50-µs waveform per IEC 62368-1	4077	8700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in air or oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	5300	11312	V_{PK}
q_{pd}	Apparent charge[4]	Method a, After input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	≤ 5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s (S) $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s (G/W)	≤ 5	≤ 5	
		Method b1, At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s (S) $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s (G/W)	≤ 5	≤ 5	
C_{IO}	Barrier capacitance, input to output[5]	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1MHz	~ 0.5	~ 0.5	pF
R_{IO}	Isolation resistance[5]	V_{IO} = 500V, T_A = 25°C	$> 10^{12}$	$> 10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	$> 10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$> 10^{9}$	$> 10^{9}$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production)	3750	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

7.7 Safety-Related Certifications

VDE	UL (Pending)	CQC
Certified according to DIN EN IEC60747-17(VDE 0884-17):2021-10; EN IEC60747-17:2020+AC:2021	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2022
Basic Isolation (SOIC8): V_{IORM}: 566V_{PK} V_{IOTM}: 5300V_{PK} V_{IOSM}: 5300V_{PK} Reinforced Isolation (SOIC8-WB/SOIC16-WB): V_{IORM}: 1414V_{PK} V_{IOTM}: 7070V_{PK} V_{IOSM}: 11312V_{PK}	Single protection SOIC8: 3750V_{RMS} SOIC8-WB: 5000V_{RMS} SOIC16-WB: 5000V_{RMS}	SOIC8-WB: Reinforced Insulation （Altitude ≤ 5000m）
Certification Number Reinforced Isolation Certificate: 40057278 Basic Isolation Certificate: 40052786	Certification Number:	Certification Number SOIC8-WB: CQC24001434134

7.8 Electrical Characteristics

7.8.1 V_{DDA} = V_{DDB} = 5V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = -4mA; See Figure 8- 1	V_{DDO}[1] - 0.4	V_{DDO}[1] - 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA; See Figure 8- 1		0.2	0.4	V
$V_{IT+(IN)}$	Logic input high level threshold		0.7 × V_{DDI}[1]			V
$V_{IT-(IN)}$	Logic input low level threshold				0.3 × V_{DDI}[1]	V
I_{IH}	High-Level input leakage current	V_{IH} = V_{DDI}[1] at VIx			20	µA
I_{IL}	Low-Level input leakage current	V_{IL} = 0V at VIx	–20			µA
Z_O	Output impedance[2]			50		Ω
CMTI	Common mode transient immunity	V_I = V_{DDI}[1] or 0V, V_{CM} = 1200V; See Figure 8- 3	100	150		kV/µs
C_I	Input capacitance[3]	V_I = V_{DD}/2 + 0.4 × sin(2πft), f = 1MHz, V_{DD} = 5V		2		pF

NOTE:
1. V_{DDI} = input-side VDD supply voltage, V_{DDO} = output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50Ω ± 40%.
3. Measured from pin to Ground.

7.8.2 V_{DDA} = V_{DDB} = 3.3V ± 10%, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2mA; See Figure 8- 1	V_{DDO}[1] - 0.4	V_{DDO}[1] - 0.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2mA; See Figure 8- 1		0.2	0.4	V
$V_{IT+(IN)}$	Logic input high level threshold		0.7 × V_{DDI}[1]			V
$V_{IT-(IN)}$	Logic input low level threshold				0.3 × V_{DDI}[1]	V
I_{IH}	High-Level input leakage current	V_{IH} = V_{DDI}[1] at VIx			20	µA
I_{IL}	Low-Level input leakage current	V_{IL} = 0V at VIx	–20			µA
Z_O	Output impedance[2]			50		Ω
CMTI	Common mode transient immunity	V_I = V_{DDI}[1] or 0V, V_{CM} = 1200V; See Figure 8- 3	100	150		kV/µs
C_I	Input capacitance[3]	V_I = V_{DD}/2 + 0.4 × sin(2πft), f = 1MHz, V_{DD} = 3.3V		2		pF

NOTE:
1. V_{DDI} = input-side VDD supply voltage, V_{DDO} = output-side VDD supply voltage.
2. The nominal output impedance of each isolator driver is 50Ω ± 40%.
3. Measured from pin to Ground.

7.9 Supply Current

7.9.1 V_{DDA} = V_{DDB} = 5V ± 10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ZMCIS3720C							
Supply Current – DC Signal	V_{IN} = 0V (ZMCIS3720CL); V_{IN} = V_{DDI}[1] (ZMCIS3720CH)		I_{DDA}		1.0	2.1	mA
			I_{DDB}		2.9	5.0	
	V_{IN} = V_{DDI}[1] (ZMCIS3720CL); V_{IN} = 0V (ZMCIS3720CH)		I_{DDA}		3.8	6.3	
			I_{DDB}		3.1	5.3	
Supply Current – AC Signal	All channels switching with 5V, 50% duty cycle square wave clock input; C_L = 15pF for each channel.	1Mbps (500kHz)	I_{DDA}		2.5	4.4	
			I_{DDB}		3.1	5.3	
		10Mbps (5MHz)	I_{DDA}		3.0	5.1	
			I_{DDB}		3.9	6.5	
		40Mbps (20MHz)	I_{DDA}		3.4	5.7	
			I_{DDB}		6.5	10.4	
ZMCIS3721C							
Supply Current – DC Signal	V_{IN} = 0V (ZMCIS3721CL); V_{IN} = V_{DDI}[1] (ZMCIS3721CH)		I_{DDA}		1.8	3.4	mA
			I_{DDB}		1.9	3.5	
	V_{IN} = V_{DDI}[1] (ZMCIS3721CL); V_{IN} = 0V (ZMCIS3721CH)		I_{DDA}		3.3	4.9	
			I_{DDB}		3.4	5.0	
Supply Current – AC Signal	All channels switching with 5V, 50% duty cycle square wave clock input; C_L = 15pF for each channel.	1Mbps (500kHz)	I_{DDA}		2.6	5.4	
			I_{DDB}		2.7	5.5	
		10Mbps (5MHz)	I_{DDA}		3.3	6.5	
			I_{DDB}		3.4	6.6	
		40Mbps (20MHz)	I_{DDA}		5.3	9.5	
			I_{DDB}		5.4	9.6	
ZMCIS3722C							
Supply Current – DC Signal	V_{IN} = 0V (ZMCIS3722CL); V_{IN} = V_{DDI}[1] (ZMCIS3722CH)		I_{DDA}		1.8	3.4	mA
			I_{DDB}		1.9	3.5	
	V_{IN} = V_{DDI}[1] (ZMCIS3722CL); V_{IN} = 0V (ZMCIS3722CH)		I_{DDA}		3.3	4.9	
			I_{DDB}		3.4	5.0	
Supply Current – AC Signal	All channels switching with 5V, 50% duty cycle square wave clock input; C_L = 15pF for each channel.	1Mbps (500kHz)	I_{DDA}		2.6	5.4	
			I_{DDB}		2.7	5.5	
		10Mbps (5MHz)	I_{DDA}		3.3	6.5	
			I_{DDB}		3.4	6.6	
		40Mbps (20MHz)	I_{DDA}		5.3	9.5	
			I_{DDB}		5.4	9.6	

NOTE:

1. V_{DDI} = input-side VDD supply voltage.

7.9.2 $V_{DDA} = V_{DDB}$ = 3.3V ± 10%, T_A = -40 to 125°C

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ZMCIS3720C							
Supply Current – DC Signal	V_{IN} = 0V (ZMCIS3720CL); $V_{IN} = V_{DDI}$[1] (ZMCIS3720CH)		I_{DDA}		1.0	2.1	mA
			I_{DDB}		2.8	4.8	
	$V_{IN} = V_{DDI}$[1] (ZMCIS3720CL); V_{IN} = 0V (ZMCIS3720CH)		I_{DDA}		3.7	6.2	
			I_{DDB}		3.0	5.1	
Supply Current – AC Signal	All channels switching with 3.3V, 50% duty cycle square wave clock input; C_L = 15pF for each channel.	1Mbps (500kHz)	I_{DDA}		2.4	4.2	
			I_{DDB}		3.0	5.1	
		10Mbps (5MHz)	I_{DDA}		2.8	4.8	
			I_{DDB}		3.4	5.7	
		40Mbps (20MHz)	I_{DDA}		3.2	5.4	
			I_{DDB}		5.0	8.7	
ZMCIS3721C							
Supply Current – DC Signal	V_{IN} = 0V (ZMCIS3721CL); $V_{IN} = V_{DDI}$[1] (ZMCIS3721CH)		I_{DDA}		1.8	3.2	mA
			I_{DDB}		1.8	3.2	
	$V_{IN} = V_{DDI}$[1] (ZMCIS3721CL); V_{IN} = 0V (ZMCIS3721CH)		I_{DDA}		3.1	4.9	
			I_{DDB}		3.2	5.0	
Supply Current – AC Signal	All channels switching with 3.3V, 50% duty cycle square wave clock input; C_L = 15pF for each channel.	1Mbps (500kHz)	I_{DDA}		2.5	5.4	
			I_{DDB}		2.6	5.4	
		10Mbps (5MHz)	I_{DDA}		3.0	6.0	
			I_{DDB}		3.1	6.1	
		40Mbps (20MHz)	I_{DDA}		4.3	8.0	
			I_{DDB}		4.4	8.1	
ZMCIS3722C							
Supply Current – DC Signal	V_{IN} = 0V (ZMCIS3722CL); $V_{IN} = V_{DDI}$[1] (ZMCIS3722CH)		I_{DDA}		1.8	3.2	mA
			I_{DDB}		1.8	3.2	
	$V_{IN} = V_{DDI}$[1] (ZMCIS3722CL); V_{IN} = 0V (ZMCIS3722CH)		I_{DDA}		3.1	4.9	
			I_{DDB}		3.2	5.0	
Supply Current – AC Signal	All channels switching with 3.3V, 50% duty cycle square wave clock input; C_L = 15pF for each channel.	1Mbps (500kHz)	I_{DDA}		2.5	5.4	
			I_{DDB}		2.6	5.4	
		10Mbps (5MHz)	I_{DDA}		3.0	6.0	
			I_{DDB}		3.1	6.1	
		40Mbps (20MHz)	I_{DDA}		4.3	8.0	
			I_{DDB}		4.4	8.1	

NOTE:
1. V_{DDI} = input-side VDD supply voltage.

7.10 Timing Characteristics

7.10.1 $V_{DDA} = V_{DDB} = 5V \pm 10\%$, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data rate		0		40	Mbps
PW_{min}	Minimum pulse width				20	ns
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8- 1		22	35	ns
PWD	Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$			2.5	7	ns
$t_{sk(o)}$	Channel-to-Channel output skew time[1]	Same direction		1	3	ns
$t_{sk(pp)}$	Part-to-Part output skew time [2]			1	7	ns
t_r	Output signal rise time	See Figure 8- 1		2.5	4.8	ns
t_f	Output signal fall time			2.5	4.8	ns
t_{DO}	Default output delay time from input power loss	See Figure 8- 2		10	15	ns
t_{SU}	Start-up time			25	37	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

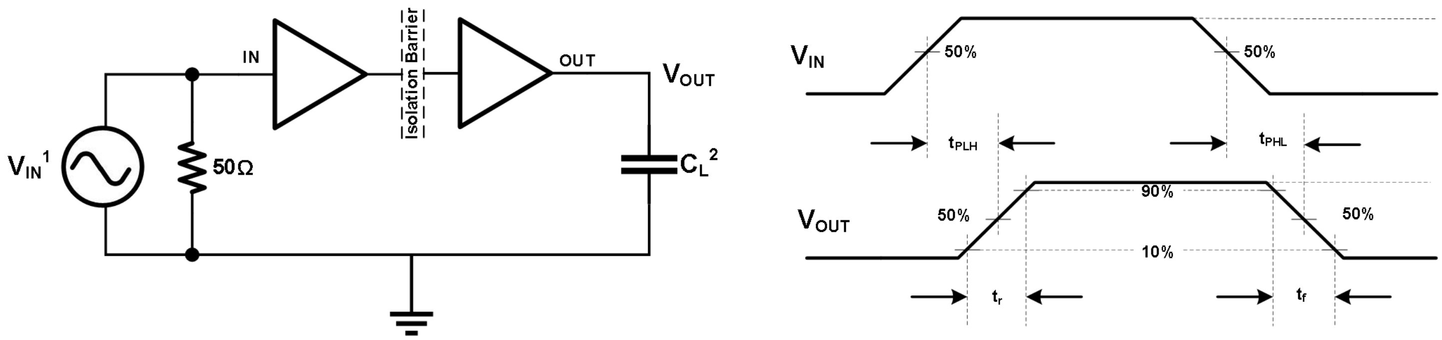
7.10.2 $V_{DDA} = V_{DDB} = 3.3V \pm 10\%$, T_A = -40 to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DR	Data rate		0		40	Mbps
PW_{min}	Minimum pulse width				20	ns
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 8- 1		22	35	ns
PWD	Pulse width distortion $\lvert t_{PLH} - t_{PHL} \rvert$			2.5	7	ns
$t_{sk(o)}$	Channel-to-Channel output skew time[1]	Same direction		1	3	ns
$t_{sk(pp)}$	Part-to-Part output skew time [2]			1	7	ns
t_r	Output signal rise time	See Figure 8- 1		2.5	4.8	ns
t_f	Output signal fall time			2.5	4.8	ns
t_{DO}	Default output delay time from input power loss	See Figure 8- 2		10	15	ns
t_{SU}	Start-up time			25	37	µs

NOTE:

1. $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
2. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

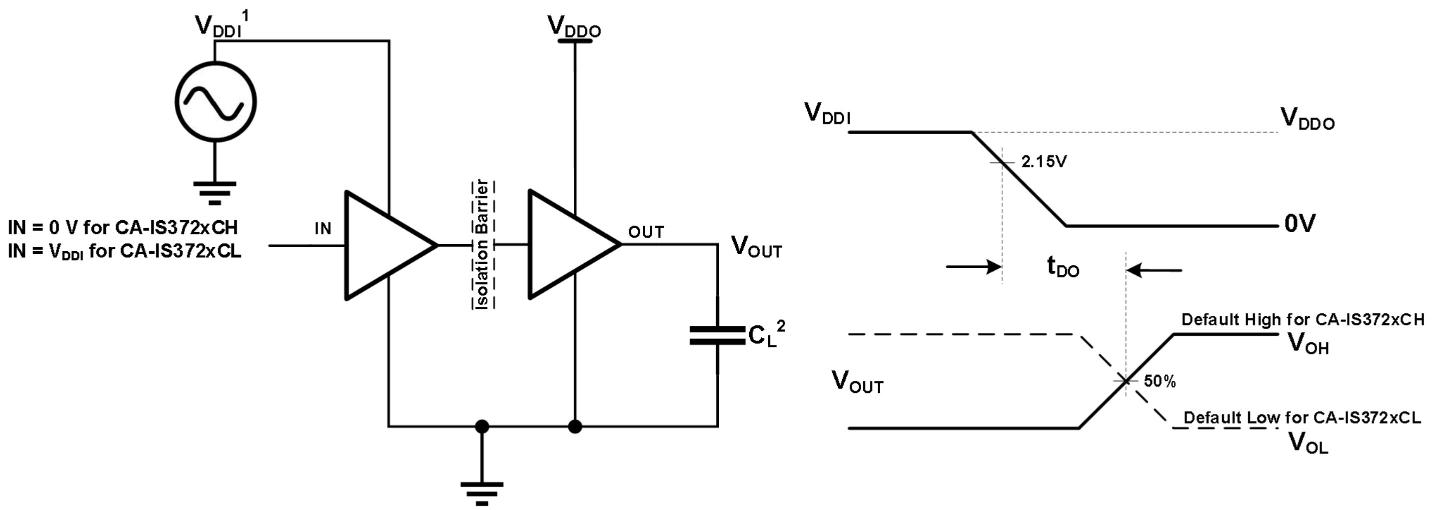
8 Parameter Measurement Information



Note:

1. A square wave generator provides V_{IN} input signal with characteristics: frequency ≤ 100kHz, 50% duty cycle, $t_r \leq 3ns$, $t_f \leq 3ns$, $Z_{out} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influences the output rising/falling time, it's a key factor in the timing characteristic measurement.

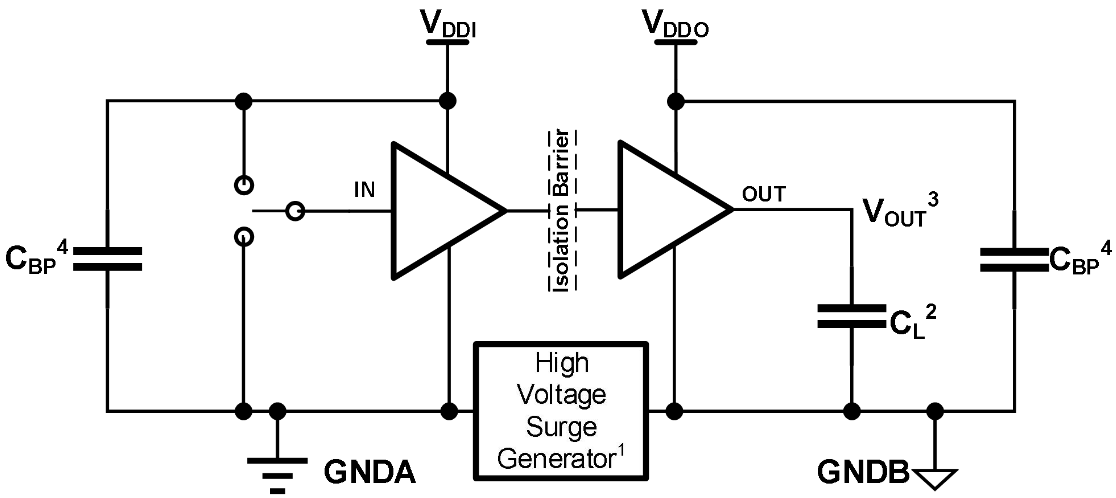
Figure 8- 1 Switching Characteristics Test Circuit and Voltage Waveforms



Note:

1. Power supply ramp rate = 10mV/ns.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influences the output rising/falling time, it's a key factor in the timing characteristic measurement.

Figure 8- 2 Default Output Delay Time Test Circuit and Voltage Waveforms



Note:
1. The High Voltage Surge Generator generates repetitive surges with > 1kV, < 10ns rise time and fall time to reach common-mode transient noise with > 100kV/µs slew rate.
2. C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
3. Pass-fail criteria: the output must remain stable whenever the high voltage surges occur.
4. C_{BP} is bypass capacitor, 0.1µF ~ 1µF.

Figure 8- 3 Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The ZMCIS372xC devices are a family of 2-channel digital galvanic isolators using Chipanalog's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovery input signal at output through a buffer stage. With this OOK architecture, the ZMCIS372xC family of devices build a robust data transmission path between different power domains, without any special start-up initialization requirements.

These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 9- 1, shows a functional block diagram of a typical channel; Figure 9- 2 shows the operating waveform of a typical channel.

9.2 Functional Block Diagram

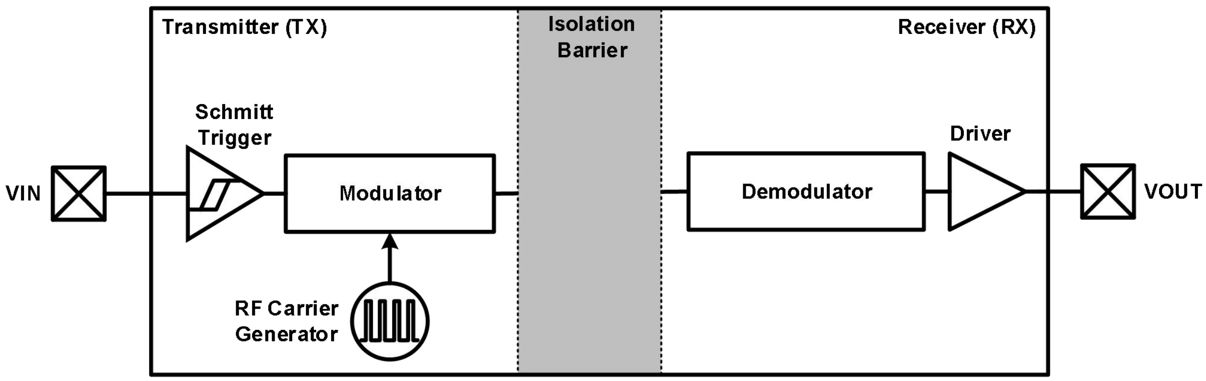


Figure 9- 1 Functional Block Diagram of a Single Channel

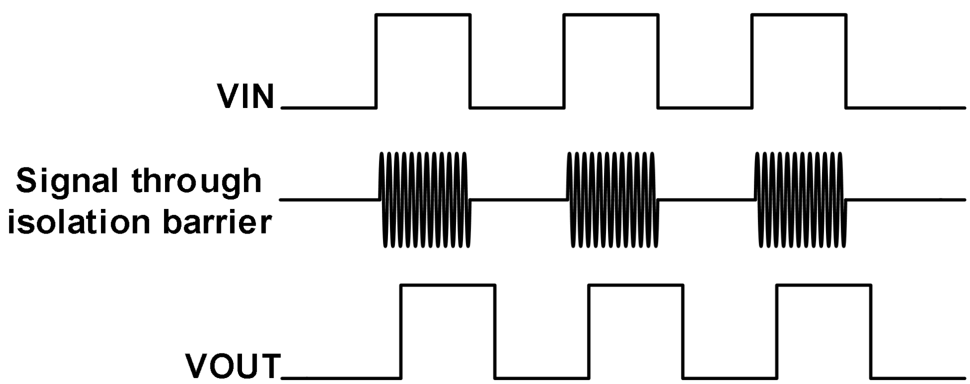


Figure 9- 2 Conceptual Operation Waveform of a Single Channel

9.3 Device Operation Modes

Table 9- 1 lists the operation modes for the ZMCIS372xC devices.

Table 9- 1 Operation Mode Table[1]

V_{DDI}[1]	V_{DDO}[1]	INPUT (VIx) [2]	OUTPUT (VOx)	OPERATION
PU	PU	H	H	Normal operation mode: A channel output follows the logic state of the input.
		L	L	
		Open	Default	Default output, fail-safe mode: If a channel input is open, the corresponding channel output goes to the default logic state (Low for ZMCIS372xCL and High for ZMCIS372xCH)
PD	PU	X	Default	Default output, fail-safe mode: When V_{DDI}[1] is unpowered, the corresponding channel output goes to the default logic state (Low for ZMCIS372xCL and High for ZMCIS372xCH)
X	PD	X	Undetermined	When V_{DDO}[2] is unpowered, the output states are undetermined.[3]

NOTE:

1. V_{DDI} = Input-side Supply V_{DD}; V_{DDO} = Output-side Supply V_{DD}; PU = Powered up ($V_{DD\_} \geq V_{DD(UVLO+)}$); PD = Powered down ($V_{DD\_} \leq V_{DD(UVLO-)}$); X = Irrelevant; H = High level; L = Low level.
2. A strongly driven input signal can weakly power the floating V_{DDI} through an internal protection diode and cause undetermined output.
3. The outputs are in undetermined state when $V_{DDI} > V_{DD(UVLO+)}$, $V_{DDO} < V_{DD(UVLO-)}$.

10 Application and Implementation

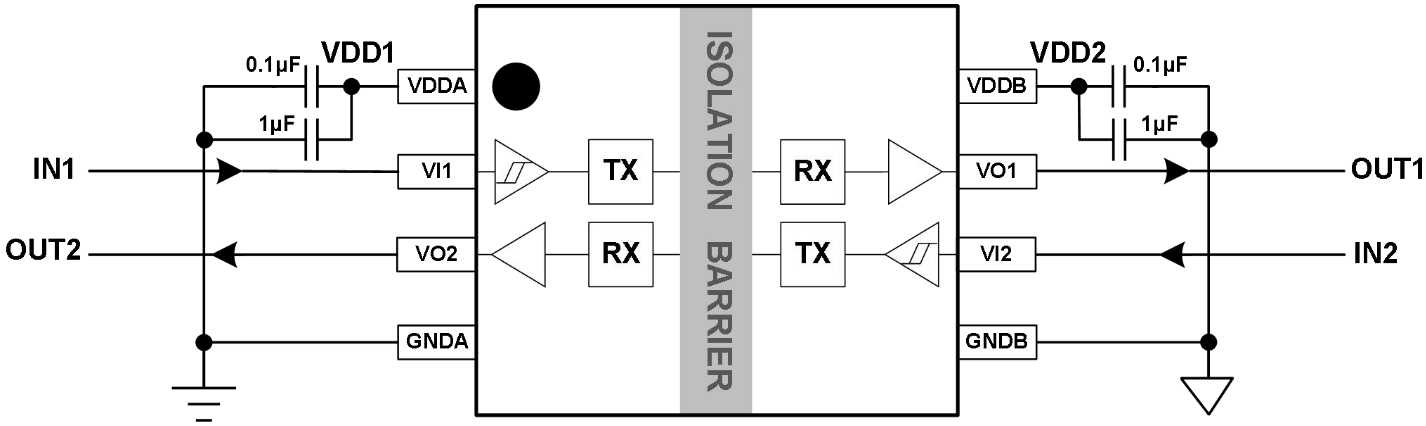


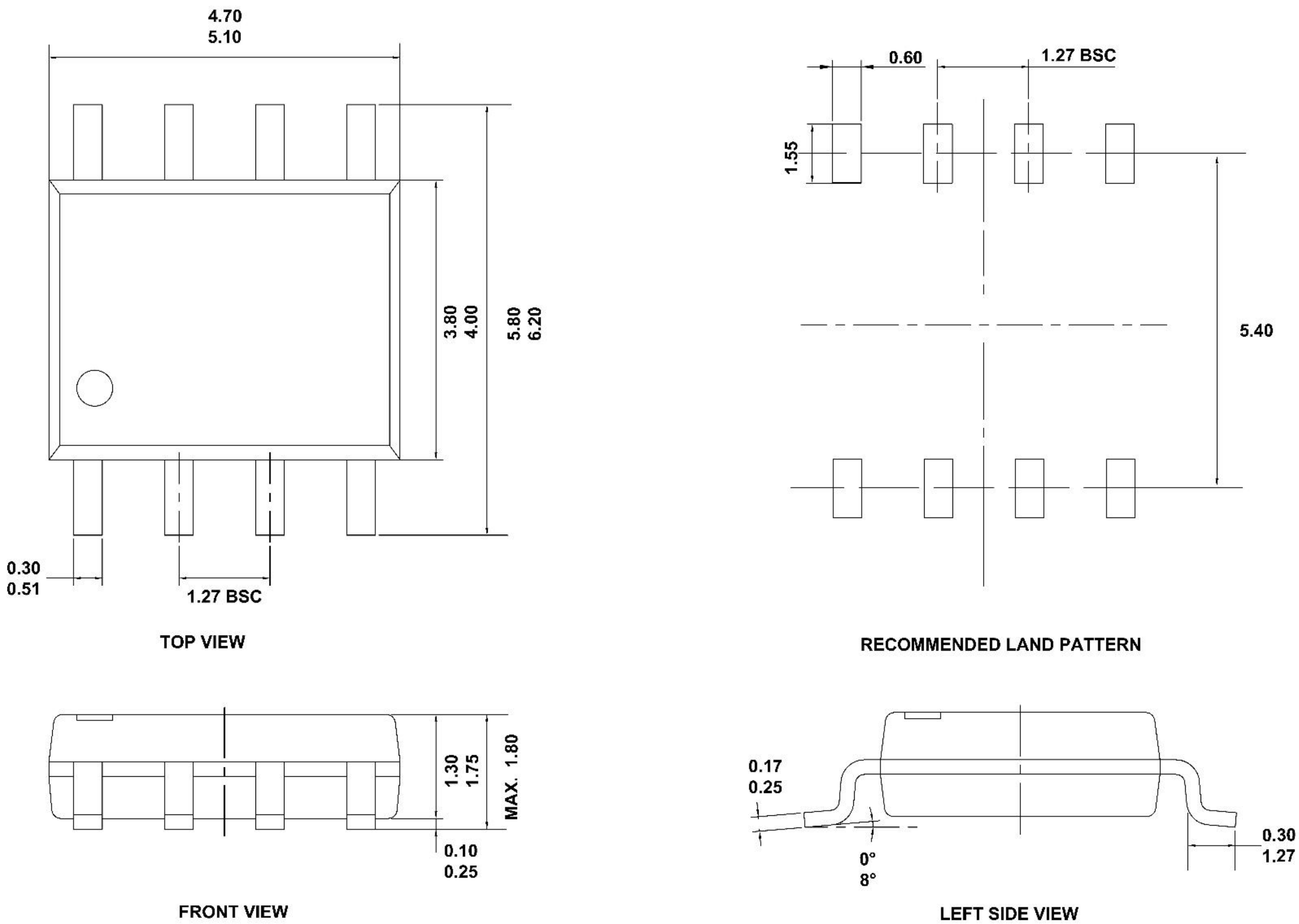
Figure 10- 1 Typical Application Circuit of ZMCIS3721Cx

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ZMCIS372xC devices only require several external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass VDDA and VDDB pins with 0.1μF to 1μF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible. Figure 10- 1 shows typical operating circuit of the ZMCIS372xC devices.

11 Package Information

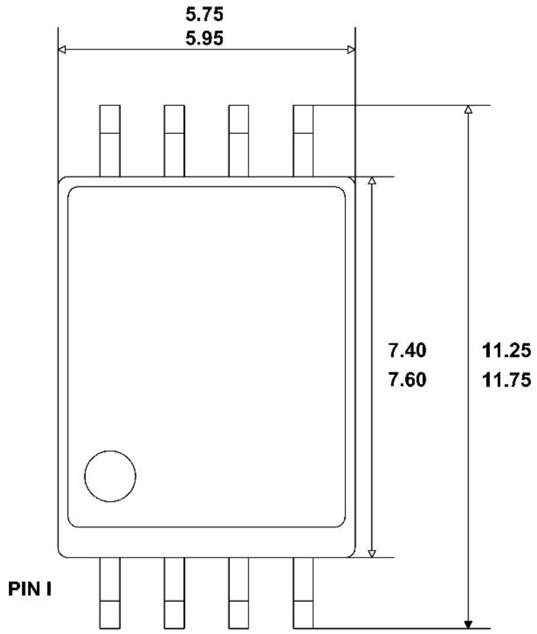
11.1 SOIC8 Package

The values for the dimensions are shown in millimeters.

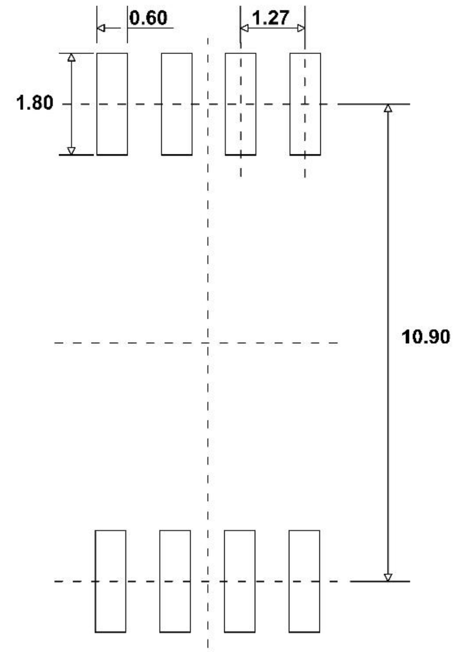


11.2 SOIC8-WB Package

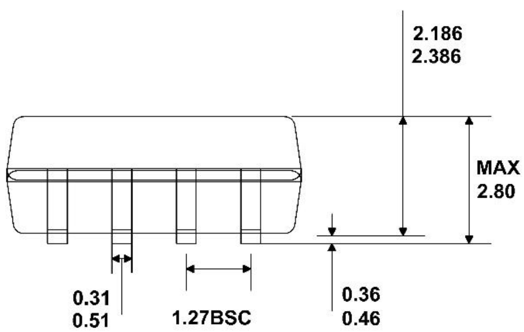
The values for the dimensions are shown in millimeters.



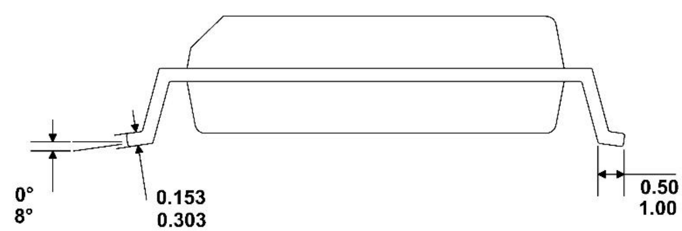
TOP VIEW



RECOMMENDED LAND PATTERN



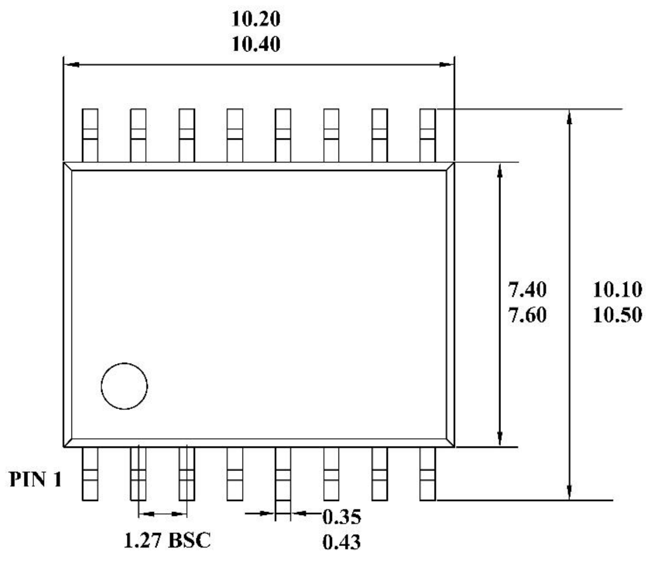
FRONT VIEW



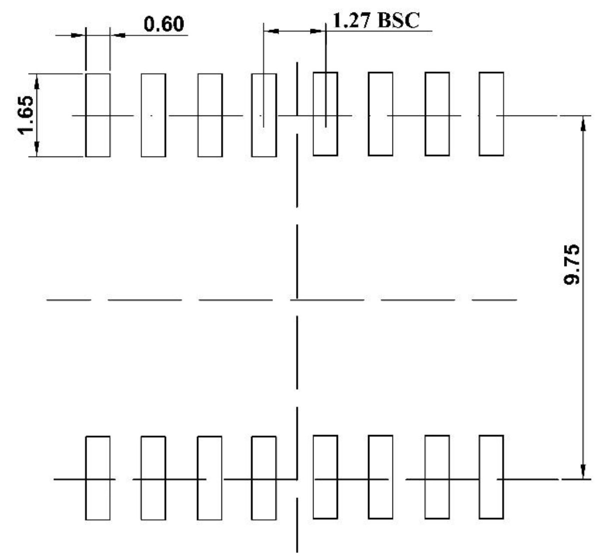
LEFT-SIDE VIEW

11.3 SOIC16-WB Package

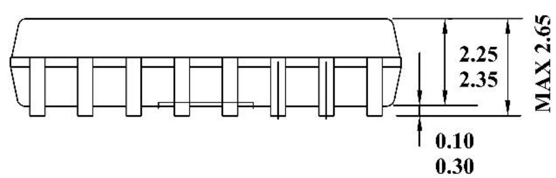
The values for the dimensions are shown in millimeters.



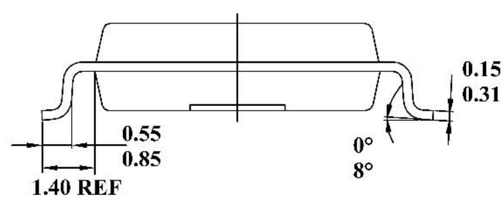
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



LEFT SIDE VIEW

12 Soldering Information

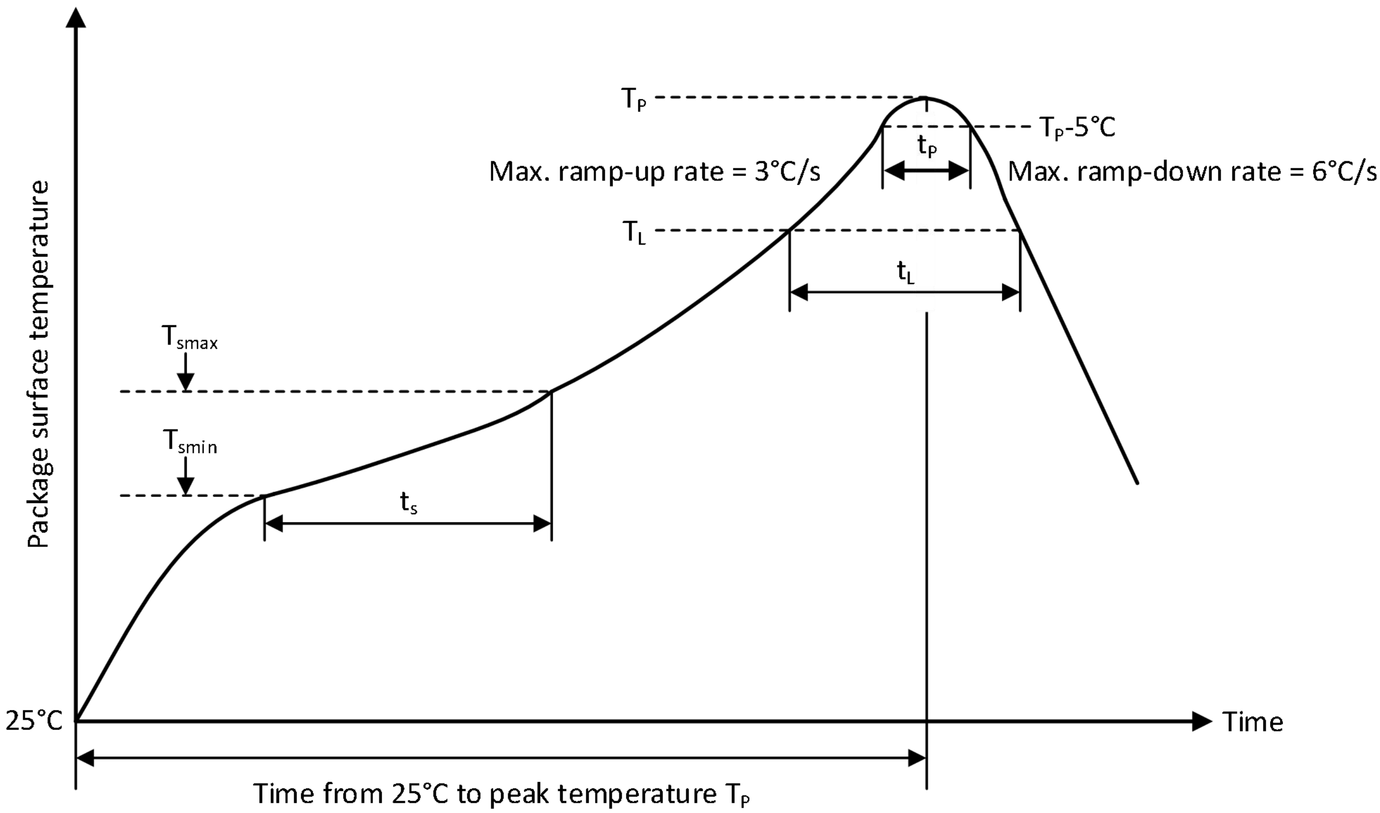


Figure 12- 1 Soldering Temperature Curve

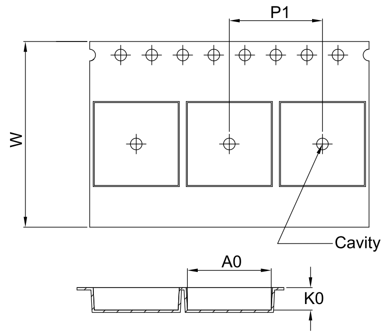
Table 12- 1 Soldering Temperature Parameters

Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

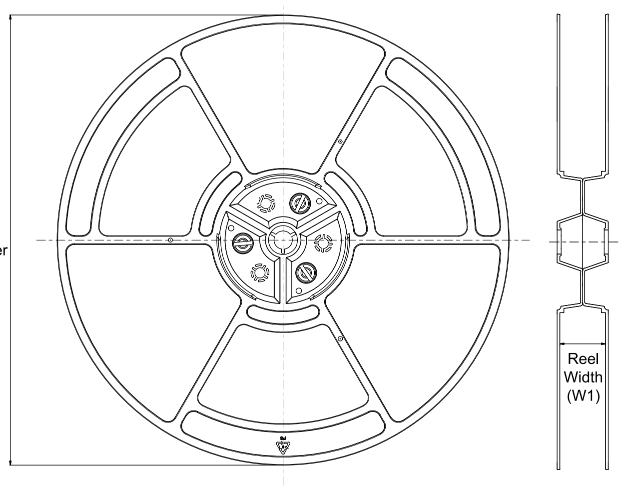
REEL DIMENSIONS

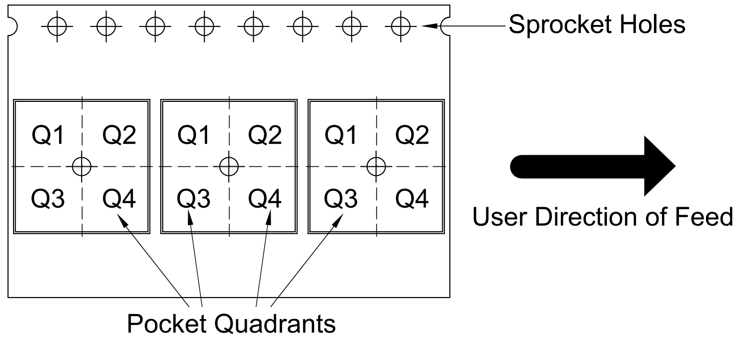
TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ZMCIS3720CLS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
ZMCIS3720CLG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
ZMCIS3720CLW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
ZMCIS3720CHS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
ZMCIS3720CHG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
ZMCIS3720CHW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
ZMCIS3721CLS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
ZMCIS3721CLG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
ZMCIS3721CLW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
ZMCIS3721CHS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
ZMCIS3721CHG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
ZMCIS3721CHW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
ZMCIS3722CLS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
ZMCIS3722CLG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
ZMCIS3722CLW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1
ZMCIS3722CHS	SOIC	S	8	2500	330	12.4	6.40	5.40	2.10	8.00	12.00	Q1
ZMCIS3722CHG	SOIC	G	8	1000	330	16.4	11.95	6.15	3.20	16.00	16.00	Q1
ZMCIS3722CHW	SOIC	W	16	1000	330	16.4	10.90	10.70	3.20	12.00	16.00	Q1